Digital-to-analog converter with gamma correction on glass substrate for TFT-panel applications

Tzu-Ming Wang (SID Student Member)
Yu-Hsuan Li
Ming-Dou Ker

Abstract — Low-temperature polysilicon (LTPS) technology has a tendency towards integrating all circuits on glass substrate. However, the poly-Si TFTs suffered poor uniformity with large variations in the device characteristics due to a narrow laser process window for producing large-grained poly-Si TFTs. The device variation is a serious problem for circuit realization on the LCD panel, so how to design reliable on-panel circuits is a challenge for system-on-panel (SOP) applications. In this work, a 6-bit R-string digital-to-analog converter (DAC) with gamma correction on glass substrate for TFT-panel applications is proposed. The proposed circuit, which is composed of a folded R-string circuit, a segmented digital decoder, and reordering of the decoding circuit, has been designed and fabricated in a 3-μm LTPS technology. The area of the new proposed DAC circuit is effectively reduced to about one-sixth compared to that of the conventional circuit for the same LTPS process.

Keywords — *Digital-to-analog converter (DAC), low-temperature polysilicon (LTPS), system-on-panel (SOP), gamma correction.*

DOI # 10.1889/JSID17.10.785

1 Introduction

Because the electron mobility of LTPS TFTs is about 100 times larger than that of conventional amorphous-silicon (a-Si) TFTs,[1] LTPS TFT-LCD technology has features such as being compact, highly reliable, and of high resolution for system integration within a display. For these features, LTPS technology is suitable for realization of system-on-panel (SOP) application and such a system integration roadmap of an LTPS TFT-LCD has been reported in the literature.[2] The distinctive feature of the LTPS TFT-LCD is the elimination of TAB ICs (integrated circuits formed by means of an interconnect technology known as tape-automated bonding). Therefore, the reliability and yield of the manufacture of a high-resolution display, and more flexibility in the design of the display system, can be further achieved.[3] LTPS TFTs can be used to manufacture complementary-metal-oxide semiconductor (CMOS) devices in the same way as in crystalline silicon-metal-oxide semiconductor field-effect transistors (MOSFETs). Figure 1 shows the cross-sectional structure of *p*-channel and *n*-channel TFTs in an LTPS process, where the *n*-channel TFT has a lightly doped drain (LDD).

The peripheral circuit blocks of the LCD panel are roughly composed of four parts – display panel, timing control circuit, scan driver circuit, and data driver circuit.[4] The display panel is composed of active-matrix liquid crystals, and the operation of the active matrices is similar to that of a DRAM (dynamic random access memory). The timing-control circuit is responsible for transmitting RGB (red, green, and blue) signals to the data driver and controlling the behavior of the scan driver. As soon as one voltage level of the scan lines rises, the RGB signals are transmitted through the data driver. After a period of time, the voltage level of this scan line is disabled and the next scan line is turned on. All voltage levels of those scan lines are raised in turn.[5]

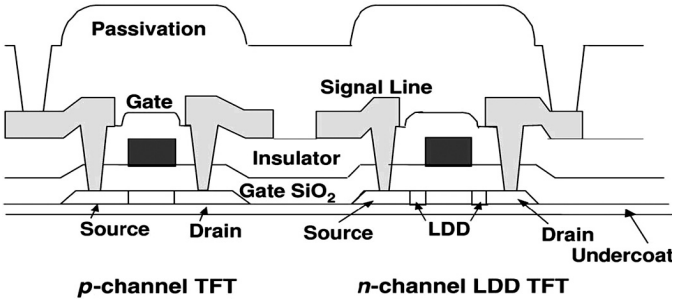

FIGURE 1 — The schematic cross-sectional view of device structures of a *p*-channel TFT and *n*-channel TFT in a LTPS process. The *n*-channel TFT has a lightly doped drain (LDD).

SOP application will be implemented step by step in the future to reduce the fabrication cost. Such integration technology contributes to shortening the product lead time because the assemblage of CMOS ICs can be eliminated. Actually, this integration level has been progressing from simple digital circuits to sophisticated ones. Moreover, LTPS technology is compatible with OLED technology, which is another promising display device. Therefore, the design of driving circuits for TFT-LCDs for LTPS technology is expected in the future. In Refs. 6 and 7, the TFT devices had been reported to have large variations in the threshold voltage and device characteristics, so device-characteristic variation is a very important issue in analog-circuit

Received 04/07/2009; accepted 06/17/2009.

The authors are with National Chiao-Tung University, Department of Electronics Engineering, Rm. 307, Engineering Blvd., #4, 1001 Ta-Hsueh Rd., Hsinchu, 300 Taiwan; telephone +886-3-571-2121 ext. 54215, fax –5412, e-mail: tzuming.ee93g@nctu.edu.tw.

design in LTPS technology.[8] In this paper, a 6-bit R-string digital-to-analog converter (DAC) with gamma correction on glass substrates for TFT-panel application is proposed. The proposed DAC with a gamma-correction design can reduce the area and complexity of the DAC on glass substrate, which is beneficial for the data driver to be integrated in the peripheral area of TFT-LCD panels for the LTPS process.

2 Gamma correction and digital-to-analog converter

2.1 Gamma correction

The gamma correction of LCDs is involved due to the nonlinearity between luminance and the human visual system (HVS). The pupils of the human eyes vary automatically for a change in ambient light. For this reason, a data driver with gamma correction is necessary in TFT-LCD panels. The data driver circuit is required to compensate for the HVS's transfer function. Figure 2 shows the operation of the gamma correction for the normally white twisted-nematic (NW-TN) type LCD panel.[4] The gamma-correction system is composed of three relationships: (1) luminance *vs.* HVS brightness, (2) input digital code *vs.* pixel voltage, and (3) the voltage–transmission (*V–T*) curve of the NW-TN-type liquid crystal. In general, the input digital codes (media codes) are designed to be directly proportional to brightness in the human eye. In the data driver circuit, a DAC is used to convert the digital RGB signals to analog gray levels, so the gamma-correction system shown in Fig. 2 can be implemented by using a DAC with a specified gamma-correction transformation.

2.2 Digital-to-analog converter

Figure 3 shows a 6-bit R-string DAC circuit with switch array decoding.[9] The architecture of this DAC requires no digital decoders and is usually used in LCD data drivers because

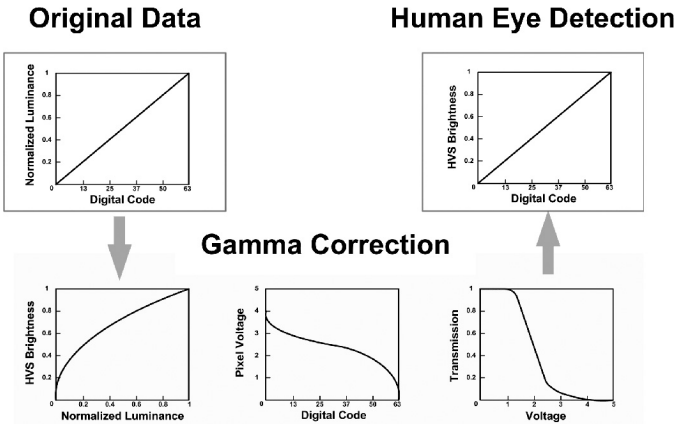

FIGURE 2 — The operation of the gamma correction for the normally white TN-type LCD panel (Ref. 5).

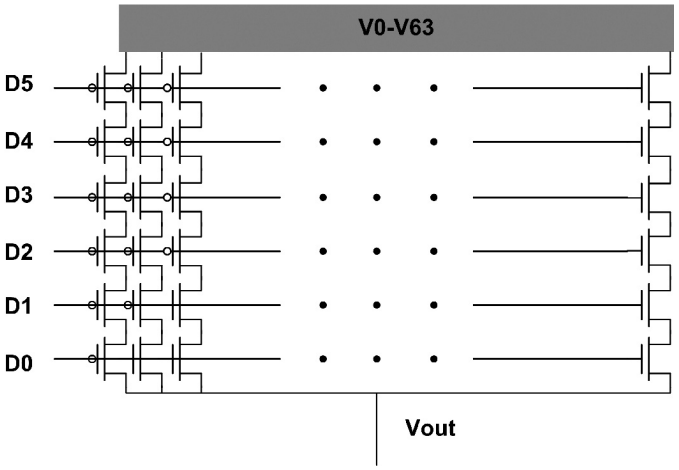

FIGURE 3 — A 6-bit R-string DAC with switch array decoding (Ref. 9).

this architecture is simple in terms of the gamma-correction design. However, the area of such a conventional switch array becomes larger and larger if the resolution of the DAC becomes higher. The load at the output node (V_{out}) also becomes larger due to the huge switch array in this conventional design.

Figure 4 shows a 6-bit R-string DAC with binary-tree decoding.[10] In opposition to the R-string DAC with switch array decoding, this circuit has less transistors in the decoding circuits. Nevertheless, the speed of this circuit is limited by the delay through the switch network. The timing skew among the switch-controlling signals often results in large glitches at V_{out}. This circuit also has a larger RC-type load at the output node (V_{out}) due to the binary-tree switches.

For higher-speed applications, Fig. 5 shows a 6-bit R-string DAC with a digital decoder.[11] The switch network is connected to the digital decoder which is controlled by a

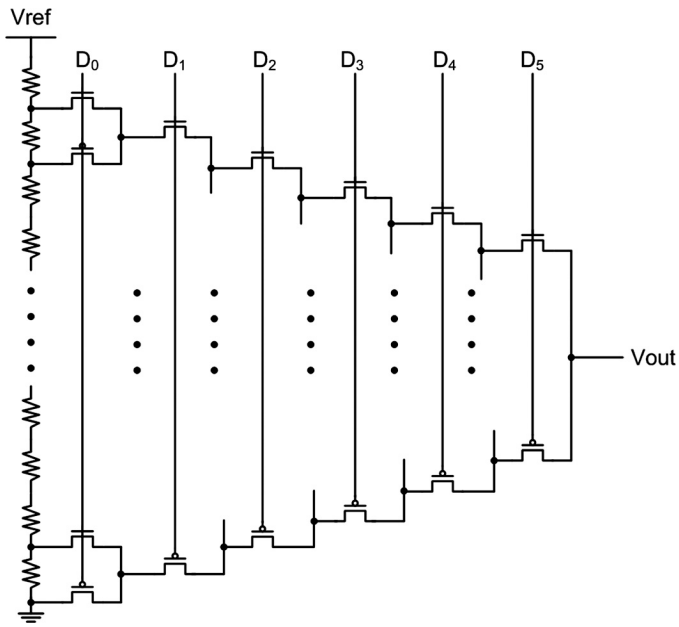

FIGURE 4 — A 6-bit R-string DAC with binary-tree decoding (Ref. 10).

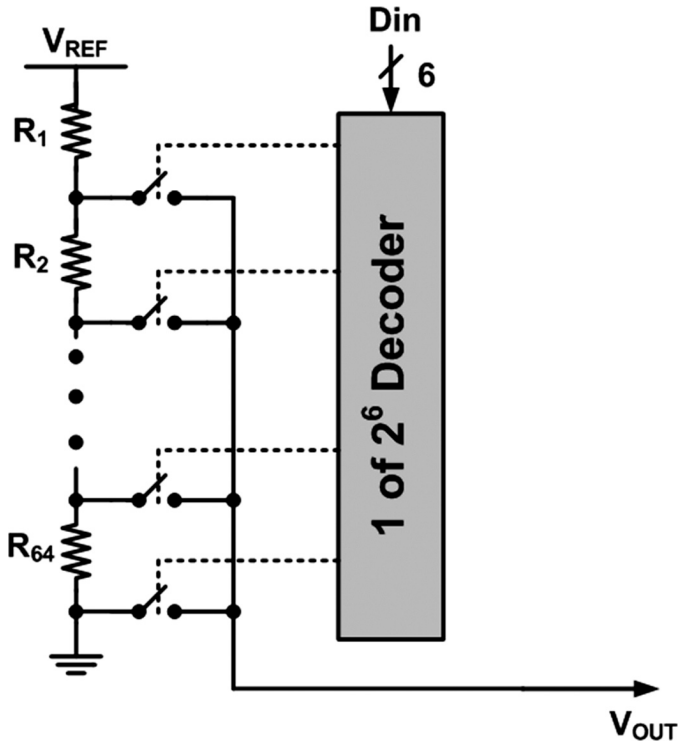

FIGURE 5 — A 6-bit R-string DAC with digital decoder (Ref. 11).

digital input code (D_{in}). The load of the output node can be reduced by the digital decoder because the output node is only connected to one column of analog switches. The operating speed of this DAC using a digital decoder is faster than that with binary-tree decoding as shown in Fig. 4. This architecture is also more suitable for gamma-correction design because it is easy to produce different sections in the resistor string. However, the area and complexity of the decoder circuits become larger and larger if the resolution becomes higher. For this reason, this R-string DAC with a digital decoder is not good enough for integrating the data driver into higher-resolution TFT-LCD panels.

As shown in Fig. 6, it is a charge-redistribution DAC.[10] The basic idea is to replace the input capacitor of a switched-capacitor (SC) gain amplifier by using a programmable capacitor array of binary-weighted capacitors. This circuit structure has some advantages over the resistor-string DAC shown in Figs. 3–5. First, the process matching for the capacitor is better than that of the resistor string. Second, charge-redistribution DAC consumes less power because it

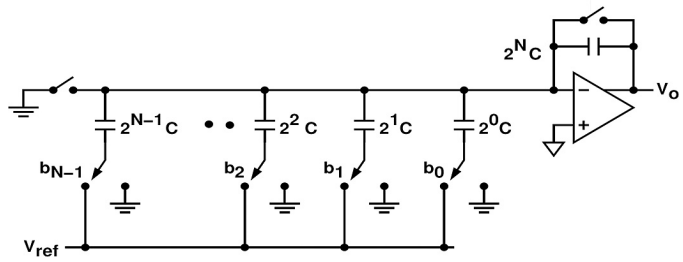

FIGURE 6 — The *n*-bit charge-redistribution DAC (Ref. 10).

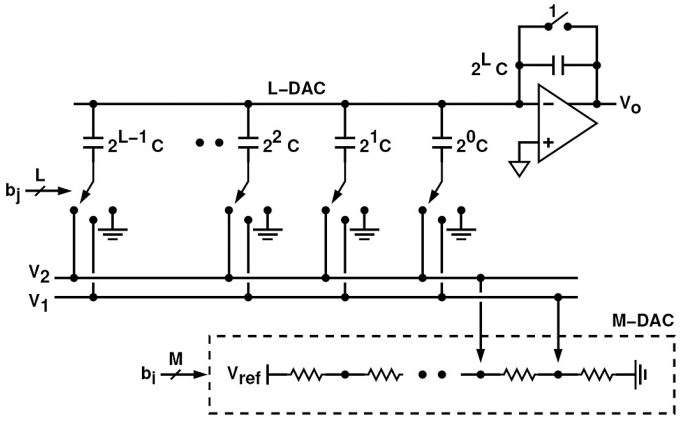

FIGURE 7 — The resistor–capacitor hybrid DAC (Ref. 15).

has no DC path in the circuit. However, for this method it is very difficult to achieve gamma correction for TFT-LCD applications. In other words, it cannot compensate the inherent characteristic of liquid crystal.

By utilizing the multiple R-string technique, DAC circuits having the advantages of higher-resolution and smaller area had been proposed.[12–14] However, by utilizing the multiple R-string technique, it is very difficult to implement the totally non-linear relationship between each gray level required for gamma-correction compensation. The first R-string divides the voltage levels non-linearly, while the second R-string divides two adjacent nodes of the first R-string again linearly. Therefore, the output voltage can not totally meet the correct voltage level in each gray level of gamma correction.

The benefits and drawbacks of resistor-string DAC and charge-redistribution DAC have been briefly discussed. A resistor–capacitor hybrid,[15] which had been proposed with benefits and without the drawbacks of the aforementioned DAC, is shown in Fig. 7. In this circuit, the upper bits are adopted in resistor-string architecture and the lower bits employ the charge-redistribution structure. This hybrid structure can achieve a higher operating speed, larger die area, and lower power consumption. Besides, it is also suitable in DACs with gamma correction. In Refs. 16–18, the performance of DAC circuits for LCD column drivers, high-speed current steering, and phase-calibrated applications is better than that of some conventional architectures of the aforementioned DAC. The reason is that the devices suffer poorer electrical characteristics and larger variations in LTPS technology compared with that for CMOS technology. Therefore, the complexity and the implementable ability are considered first in the design of the DAC circuit in LTPS technology.

3 New proposed 6-bit R-string digital-to-analog converter with gamma correction

The display transfer function is shown in Fig. 8. From the previous section, there is a non-linear relationship between luminance (luminance domain) and the human visual sys-

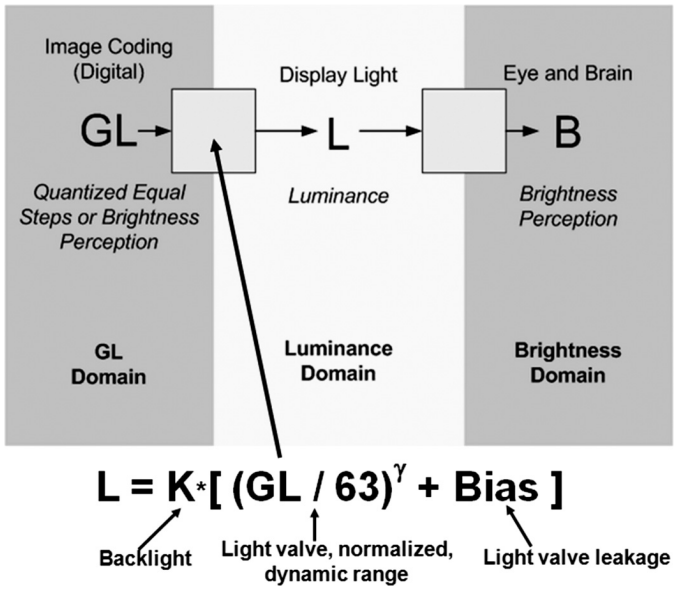

FIGURE 8 — The transform function of display system.

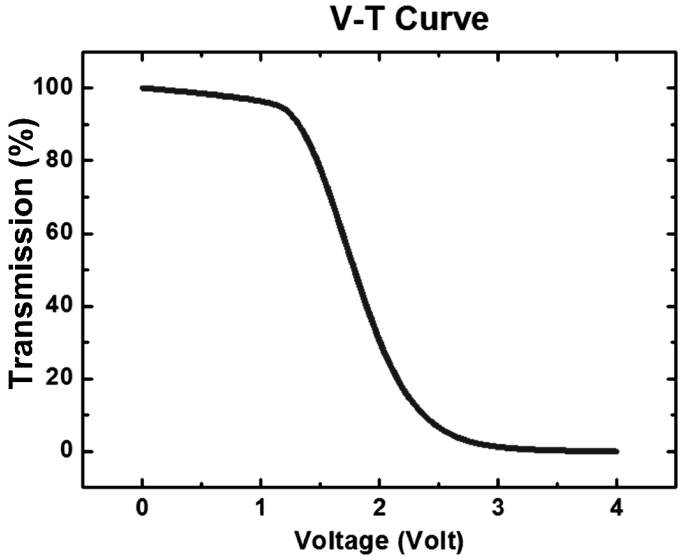

FIGURE 9 — The percentage transmission *vs.* voltage (rms) of the liquid crystal.

tem (brightness domain). For this reason, the gamma-correction design is necessary in TFT-LCD panels. The nonlinearity between the gray-level (GL) domain and the luminance domain can be corrected by implementing the gamma-correction design with the formula shown in Fig. 8. For a 6-bit gamma-correction design, the transform function for this system can be expressed as

$$\frac{T(GL)-T_{\min}}{T_{\max}-T_{\min}}=(GL/63)^{\gamma}, \tag{1}$$

$$T(GL)=(T_{\max}-T_{\min})(GL/63)^{\gamma}+T_{\min}, \tag{2}$$

$$L(GL)=T(GL)\cdot K_{backlight}, \tag{3}$$

and

$$L(GL)=(L_{\max}-L_{\min})(GL/63)^{\gamma}+L_{\min}, \tag{4}$$

where T is the transmission, GL is gray level, γ is the gamma value, and L is the luminance. From the above formula, the transform function between transmission and gray level is shown in Eq. (2). Figure 9 shows the percentage of transmission *vs.* voltage (rms) of the liquid crystal, and the liquid crystal is a normally white TN-type liquid crystal. The pixel voltage corresponding to each gray level can be obtained from the pixel voltage with a gamma value of 2.2, the transform function in Eq. (2), and the *V–T* curve of this liquid crystal.

From the above discussions, the R-string DAC with a digital decoder in Fig. 5 is a valid technique for reducing the loading of the output node. It also has a simple structure and is suitable for gamma-correction design. But this architecture has a too large area for the decoder in a high-resolution DAC. For this reason, a new architecture to reduce the area of the decoder is proposed in Fig. 10. The number of transistors in the decoder is not linearly increased but is exponentially increased with increasing the bit number. Figure 10 shows the proposed 6-bit R-string DAC with gamma correction on glass substrate for TFT-panel applications. A smaller area and lower complexity can be achieved by using this new design. The new proposed R-string DAC shown in Fig. 10 is composed of a folded R-string circuit, switch array, two identical segmented decoders, and the reordering of the decoding circuit.[19] The input signal D_{in} is segmented into two parts (MSBs and LSBs) and assigned to two identical segmented decoders. The MSBs determine the only single row to be selected through one segmented decoder while all others remain unselected. This operation connects eight adjacent resistor nodes in the selected row of the reordering of the decoding circuit. In the meanwhile, the LSBs determine one of eight resistor nodes in the selected

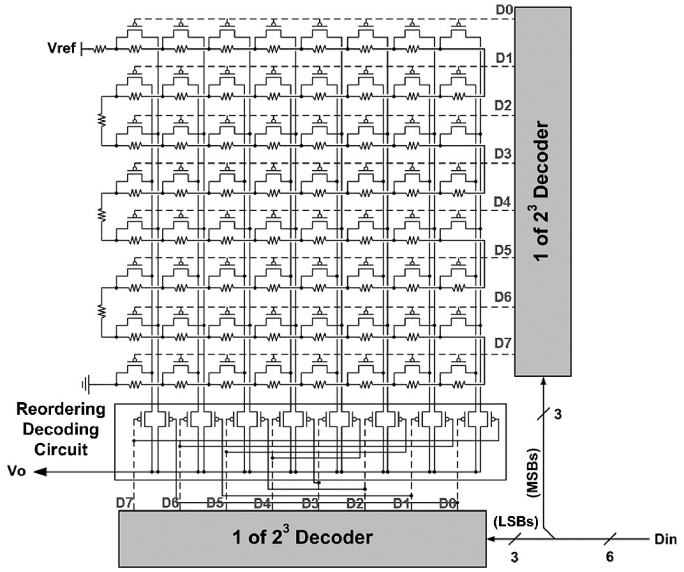

FIGURE 10 — The proposed 6-bit R-string digital-to-analog converter (DAC) with gamma correction on glass substrate for TFT-panel application.

row to be connected to the output node (V_o) through the reordering of the decodering circuit and the other segmented decoder. Therefore, the output voltage matches the correct gray level. In addition, the reordering of the decoding circuit is an important part in the proposed DAC in order to solve the function error using two identical segmented decoders. Without reordering the decoding circuit in the proposed circuit, when the LSBs of the input signal D_{in} are required to select the highest voltage level in each row, the lowest voltage level will be chosen in the even rows on the contrary, and the highest voltage level will be chosen in odd rows due to the folded R-string circuit. With the reordering of the decoding circuit, the proper voltage level can be correctly chosen to meet each gray level of gamma correction.

With the R-string approach, the DAC has guaranteed monotonicity and also has higher accuracy because the accuracy of the R-string DAC is dependent on the ratio of resistors, and not dependent on the absolute resistor values.[20] Furthermore, the area of the proposed folded R-string DAC with gamma correction can be reduced because the reordering of the decoding circuit can simplify the decoder circuit. Otherwise, the decoder connected to the LSBs has to be redesigned so the right voltage level can be chosen in even rows. Besides, the partial decoding function is replaced by the signal path routing of the reordering of the decoding circuit. The fundamental decoders can be utilized for the two identical segmented digital decoders.

The first of 2^6 decoders in the conventional design of Fig. 6 requires 64 six-input NAND gates and six inverters, while the first of 2^3 decoders in the newly proposed design of Fig. 10 only requires eight three-input NAND gates and three inverters. Therefore, the total transistors of the decoders can be decreased from 780 to 124 in such a 6-bit DAC, as compared in Fig. 11. The area of the R-string DAC can be effectively reduced to about one-sixth of that of the conventional one by using this proposed architecture. This new proposed 6-bit folded R-string DAC with segmented digital decoders is also more flexible for applying with different gamma corrections in TFT-LCD panels.

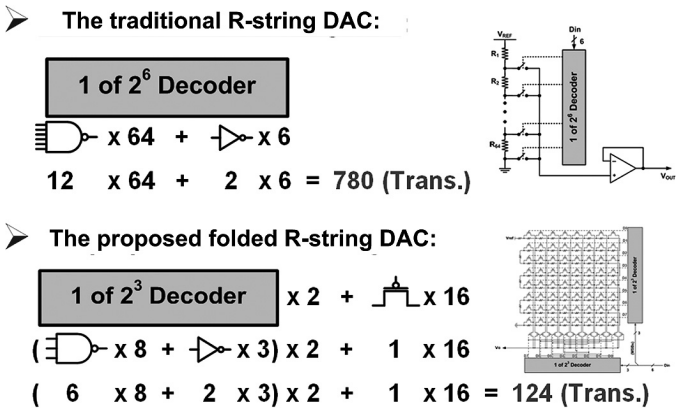

FIGURE 11 — A comparison of the number of transistors for the decoders between the conventional and proposed 6-bit R-string DAC.

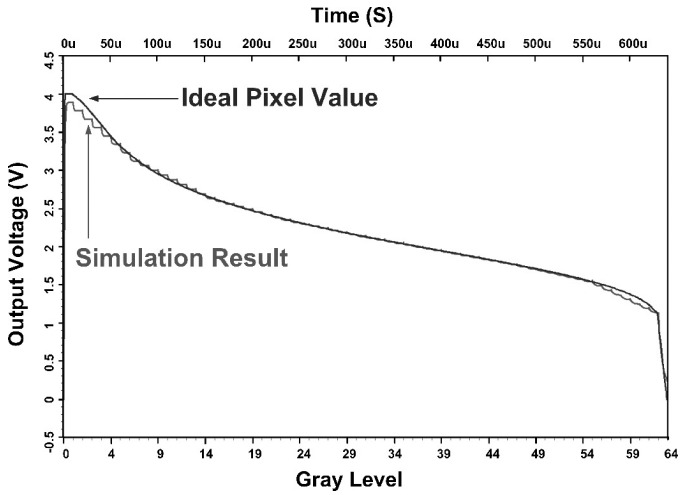

FIGURE 12 — The simulation result of 6-bit R-string digital-to-analog converter (DAC) with gamma correction in 3-μm LTPS technology at 100-kHz operation frequency.

The pixel value can be derived with a gamma value of 2.2 by using the transform function with a proper resistance ratio. The proposed DAC circuit has been fabricated by 3-μm LTPS technology. The simulation result of this DAC, assigned a series of digital input codes from 000000 (GL = 0) to 111111 (GL = 63) at 100-kHz operation frequency, is shown in Fig. 12. Around the lowest and highest gray levels, some data of the simulation result do not agree well with the ideal pixel value. The reason is that the ideal pixel value for the highest gray level is 0 while for the lowest gray level is the highest voltage value (usually is VDD). In this design of the R-string DAC, the R-string is divided into eight intervals in order to fit the ideal pixel value, and each interval is divided into the same sub-interval again. Therefore, the lowest gray level is not well-fitted to the ideal pixel value of VDD and this sub-interval also does not agree with the ideal pixel value. The similar situation happens for the highest gray level.

4 Experimental results and discussion

The proposed 6-bit R-string DAC with gamma-correction on glass substrate for TFT panel applications has been designed and fabricated in a 3-μm LTPS process. The die photo of the fabricated DAC circuit on glass substrate is shown in Fig. 13, which occupies an area of 1110 × 1180 μm. The largest resistor used in the DAC is 56.48 kΩ with an occupied layout area of 75 × 112 μm in a 3-μm LTPS process. Due to the gamma-correction design, the resistors have different values for each gray level and the total resistance used in the DAC is 199.95 kΩ. The resistor value can be adjusted according to different liquid crystals. If the output of the DAC is connected to a buffer, the resistor value can be drawn larger to reduce the power consumption from the R-string. The measured results of the output voltage in the proposed R-string DAC with gamma correction in the 3-μm LTPS process are shown in Fig. 14. With the transform

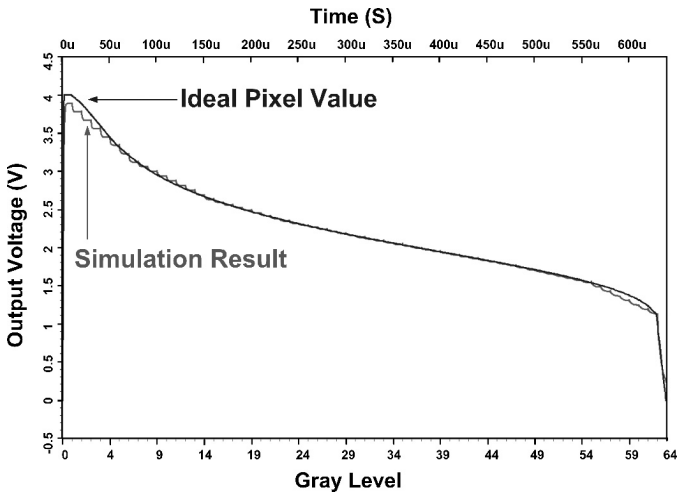

FIGURE 13 — The on-glass photo of 6-bit R-string DAC with gamma-correction realized for the 3-μm LTPS process.

function and proper resistance ratio, the measured results agree well with the simulation results with a gamma value of 2.2. The measured results are just the output of the R-string and the buffer is not included in the layout.

Although the LTPS process with enlarged poly-grain size can improve the device performance, it usually accompanies a random device-to-device variation on the LCD panel. The harmful effects of irregular grain boundaries, gate-insulator interface defects, and incomplete ion-doping activation in thin poly-Si channels often result in the variation of the electrical characteristics of LTPS TFTs.[21]

Despite the many advantages of LTPS technology, the main applications are still limited to small-sized displays. The reason is that the poly-Si TFTs have poor uniformity and suffer from large variations in the device characteristics due to the narrow laser process window for producing large-grained poly-Si thin film. The random grain boundaries and trap density exist in the channel region. This leads to some problems in real product applications such as non-uniformity brightness on the panel, error reading in the digital circuits, current gain mismatching in the analog circuits, *etc*.[6]

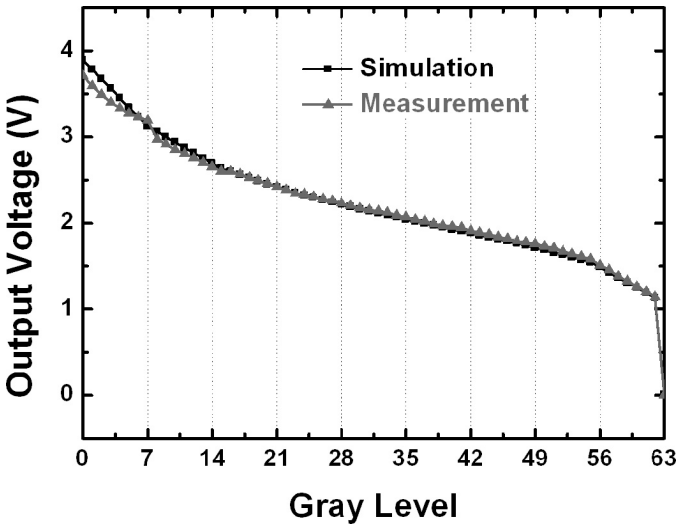

FIGURE 14 — The measured results of output voltage in the fabricated on-glass substrate R-string DAC with gamma correction for the 3-μm LTPS process.

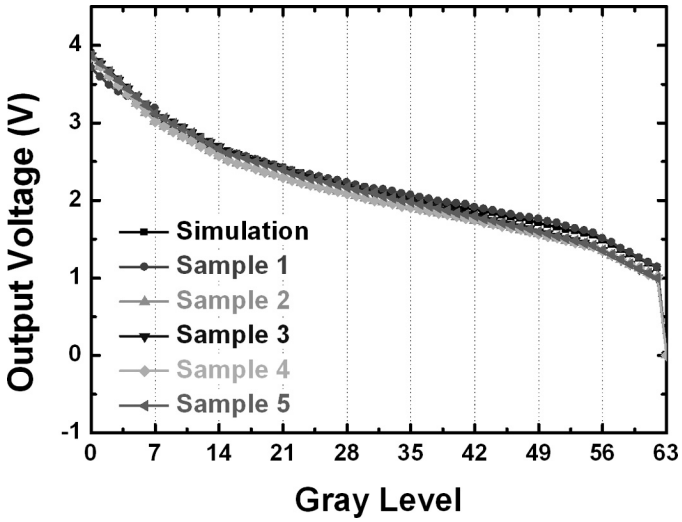

FIGURE 15 — The measured results on the output voltage among five fabricated R-string DAC samples for the 3-μm LTPS process.

Figure 15 shows the measured results of the proposed R-string DAC among five different samples. INL and DNL are two important characteristics of the DAC circuit. Integral nonlinearity (INL) is usually defined to be the deviation from a straight line, and differential non-linearity (DNL) is defined as the variation in the analog step sizes away from one LSB.[10] However, in this work, the proposed DAC circuit presents a non-linear relationship between each gray level due to gamma-correction compensation, *i.e.*, the LSB is not a constant value. Therefore, Fig. 16 shows (a) the averaged output voltage, (b) maximum error, (c) standard deviation, and (d) percentage error among five fabricated R-string DAC samples for the 3-μm LTPS process. The percentage error shown in Fig. 16 (d) is defined as

$$\frac{Simulated\_Voltage - Measured\_Voltage}{Simulated\_Voltage} \cdot 100\%. \quad (5)$$

The standard deviation and percentage error have a large difference at gray-level 63. The reason is that the simulation voltage at gray-level 63 is about 0.005 V, and the measured voltage in five different samples are 0.002, 0.006, 0.003, 0.005, and 0.005, respectively. The variation of each sample is due to the non-uniformly resistor doping. To eliminate the variation on each sample, the calibration cir-

TABLE 1 — Performance comparison among this work and some prior articles.

	This work	Ref. 14	Ref. 16
Technology	3-μm LTPS	2-μm LTPS	0.35-μm CMOS
Power supply	4 V	N/A	5 V
Number of bits	6	8	10
Maximum DNL	shown in Fig. 20	< 1 LSB	3.83 LSB
Maximum INL	shown in Fig. 20	N/A	3.84 LSB
Settling time	< 20 μsec	N/A	3 μsec
Power consumption	82 μW	N/A	3 μA/buffer
Area	1110 × 1180 μm	3 × 30.24 mm for DAC and digital logic	0.2 × 1.26 mm for four channels

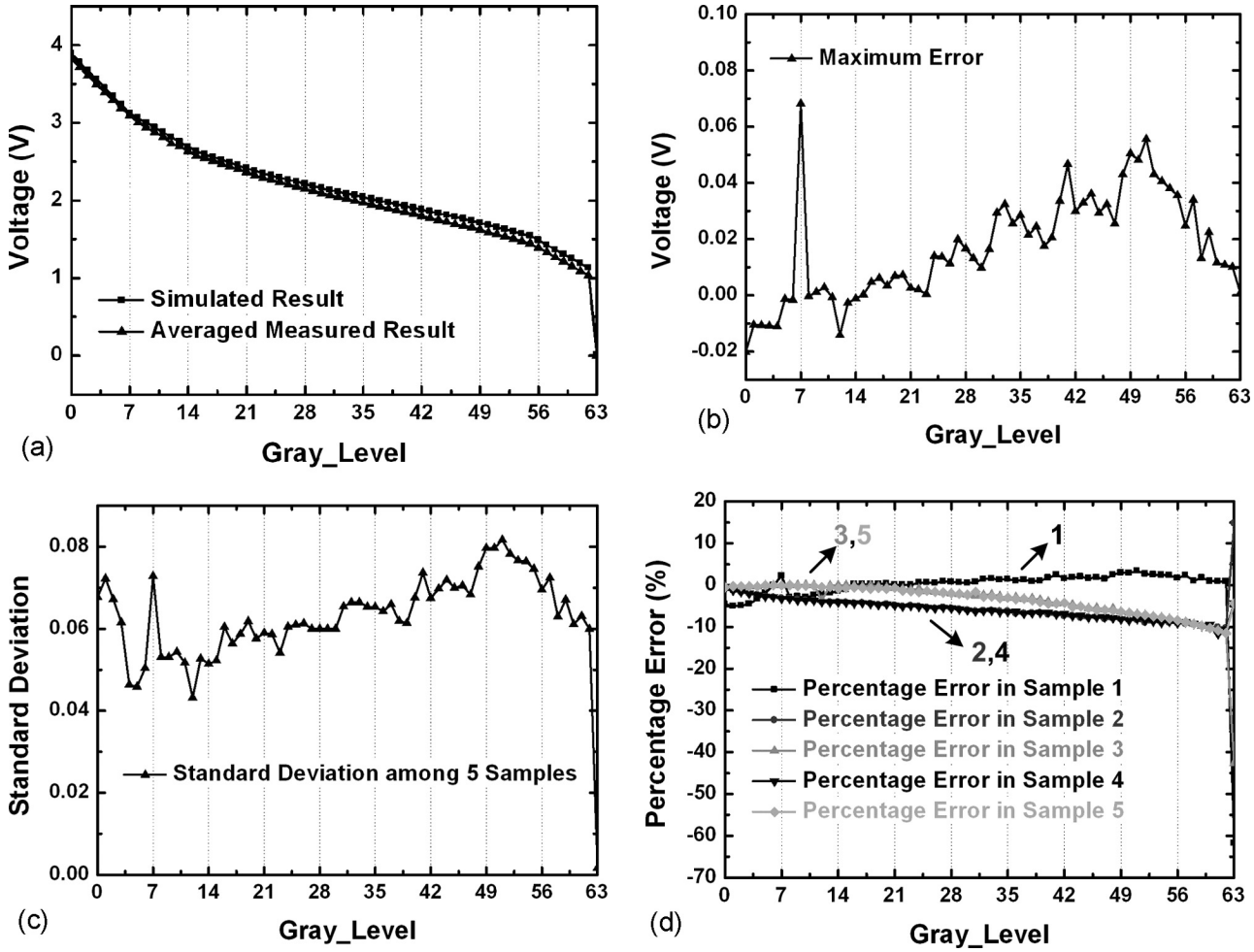

FIGURE 16 — (a) The averaged output voltage, (b) maximum error, (c) standard deviation, and (d) percentage error in five fabricated R-string DAC samples for the 3-μm LTPS process.

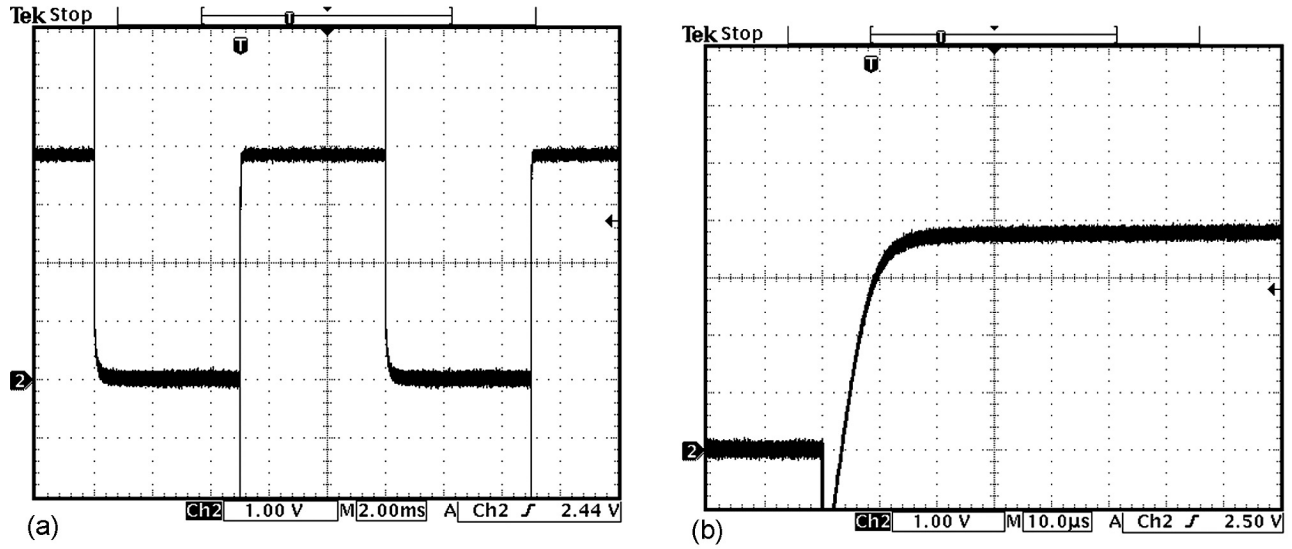

FIGURE 17 — (a) Measured output waveform when digital codes vary from 000000 to 111111 at 100 Hz and (b) measured output waveform for settling-time evaluation.

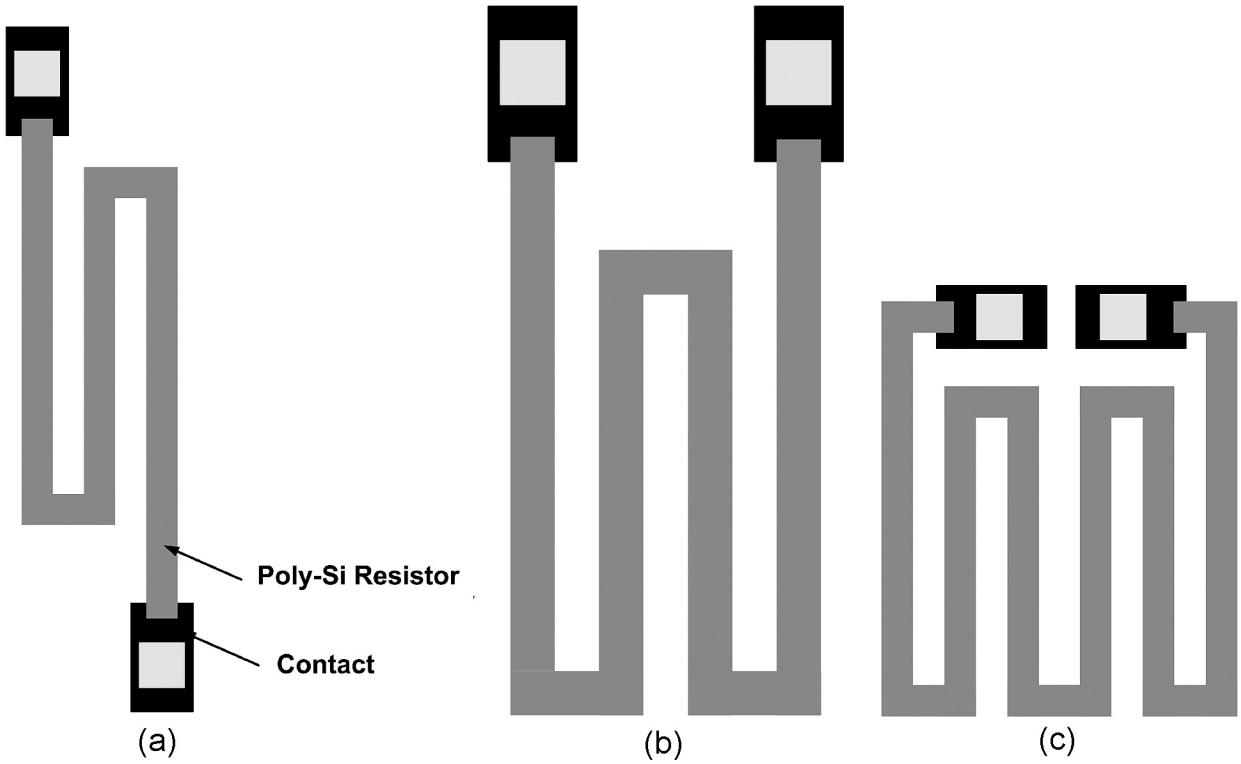

FIGURE 18 — Three different layouts to realize resistor on glass substrate.

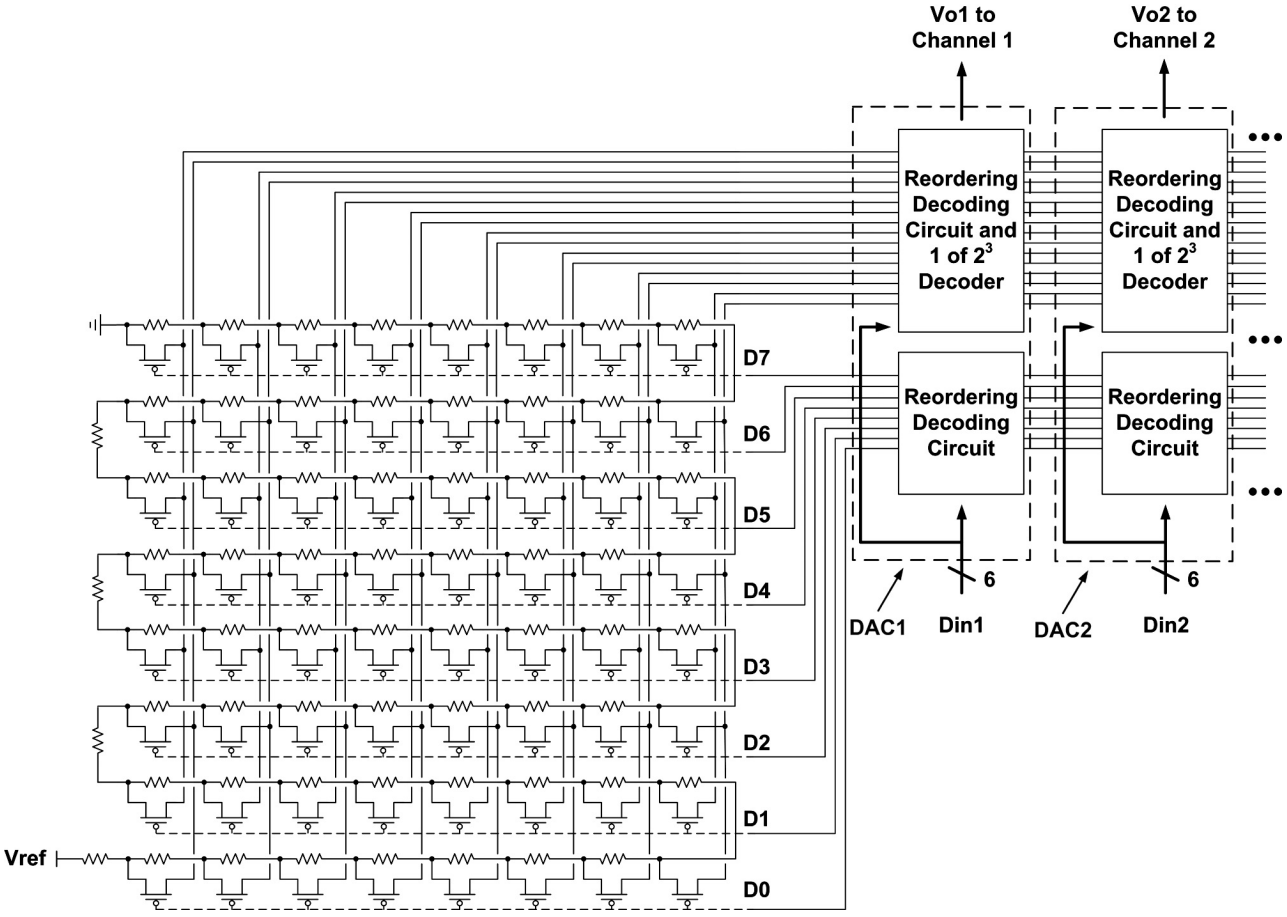

FIGURE 19 — Suggested layout arrangement of the proposed circuit with shared R-string for multiple channels in LTPS TFT panels.

cuit or layout optimization should be developed.[22] Figure 17(a) shows the measured output waveform when digital codes vary from 000000 to 111111 at 100 Hz, and Fig. 17(b) shows the measured output waveform for settling time evaluation. In Fig. 17(b), the settling time is within 20 μsec when the output node (V_o) is directly connected to the oscilloscope; therefore, the output loading is about 10 pF due to the voltage probe. The performance comparison among this work and some prior arts are summarized in Table 1. INL and DNL cannot be directly derived due to the non-linear relationship between each gray level for gamma-correction compensation. Therefore, Fig. 16 shows the numerical analysis of the measured data.

Figure 18 shows three different resistor layouts. The two contacts of a serpentine resistor should reside as close to one another as possible to minimize the impact of thermoelectrics. Figure 18(a) has unnecessarily large thermal variations due to an excessive separation between its contacts. In Fig. 18(b), the layout reduces thermal variability and improves matching by bringing the resistor heads into closer proximity. However, this layout is vulnerable to misalignment errors. Figure 18(c) eliminates the misalignment vulnerability. Besides, the trimming technique[23] used in the bandgap reference circuit can be further adopted to obtain the precise output voltage for this DAC on glass substrate.

Finally, the R-string is often shared by several output channels for TFT-panel applications, so the routing will be complex. Therefore, the occupied layout area and location should be optimized in commercial TFT panels. In this work, the optimization of the layout area and location of the DAC is not well designed because the main purpose of this work is to verify the function and performance of the DAC implemented in the LTPS process. For commercial TFT-panel applications, one suggested layout arrangement is shown in Fig. 19 where the R-String is shared by several DACs and each DAC is composed of only two decoders and one reordering circuit. In addition, the output of each DAC (V_o) will be connected to each channel correspondingly. The control signals for each DAC are in parallel with each other, so the DAC can be simply duplicated for several channels with the shared R-string.

5 Conclusion

A 6-bit folded R-string DAC with gamma correction on glass substrate has been successfully designed and verified for 3-μm LTPS technology. By using the folded R-string circuit, segmented digital decoders, and reordering the decoding circuit, the area of the newly proposed DAC circuit can be effectively reduced to about one-sixth of that of the conventional DAC circuit. Furthermore, the proposed architecture is also more flexible for gamma correction design for different LTPS processes by modifying the corresponding R-string value and the decoder. With more analog and digital circuits realized on the glass substrate in LTPS technology, the goal of system-on-panel (SOP) applications can be achieved in the near future.

Acknowledgment

This work was supported by AU Optronics Corp. and particularly supported by the "Aim for the Top University Plan" of National Chiao Tung University and Ministry of Education, Taiwan, R.O.C.

References

1 S. Uchikoga, "Low-temperature polycrystalline silicon thin-film transistor technologies for system-on-glass displays," *MRS Bulletin,* 881–886 (Nov. 2002).
2 Y. Nakajima *et al.,* "Ultra-low-power LTPS TFT-LCD technology using a multi-bit pixel memory circuit," *SID Symposium Digest* **37**, No. 4, 1185–1188 (2006).
3 Y. Nakajima *et al.,* "Latest development of 'System-on-Glass' display with low temperature poly-Si TFT," *SID Symposium Digest* **35**, No. 3, 864–867 (2004).
4 Y.-H. Tai, *Design and Operation of TFT-LCD Panels* (Wu-Nan Book, Inc., 2006).
5 E. Lueder, *Liquid Crystal Displays Addressing Schemes and Electro-Optical Effects* (John Wiley and Sons, Inc., 2004).
6 M.-D. Ker *et al.,* "On-panel output buffer with offset compensation technique for data driver in LTPS technology," *IEEE J. Display Technol.* **2**, No. 2, 153–159 (2006).
7 W.-Y. Guo *et al.,* "Reliability of low temperature poly-Si thin film transistor," *IDMC Tech. Digest* (2003).
8 S.-C. Huang *et al.,* "Statistical investigation on the variation behavior of low-temperature poly-Si TSTs for circuit simulation," *SID Symposium Digest* **37**, 329–332 (2006).
9 P. R. Gray *et al., Analysis and Design of Analog Integrated Circuits* (John Wiley & Sons, Inc., 2001).
10 D. Johns and K. Martin, *Analog Integrated Circuit Design* (John Wiley & Sons, Inc., 1997).
11 P. E. Allen and D. R. Holberg, *CMOS Analog Circuit Design* (Oxford University Press, New York, 2002).
12 J.-Y. Hu and W.-T. Sun, "Method for reducing spikes in a digital-to-analog converter," U.S. Patent 6819277 (Nov. 16, 2004).
13 G. Panov and M. Bachhuber, "High-resolution digital-to-analog converter with a small area requirement," U.S. Patent 0195098 (Jan. 14, 2005).
14 Y.-S. Park *et al.,* "An 8b source driver for 2.0 inch full-color active-matrix OLEDs made with LTPS TFTs," *IEEE Intl. Solid-State Circuits Conf. Dig. Tech. Papers,* 130–132 (2007).
15 J. W. Yang and K. W. Martin, "High-resolution low-power CMOS D/A converter," *IEEE J. Solid-State Circuits* **24**, 1458–1461 (Oct. 1989).
16 C.-W. Lu and L.-C. Huang, "A 10-bit LCD column driver with piecewise linear digital-to-analog converters," *IEEE J. Solid-State Circuits* **43**, No. 2, 371–378 (Feb. 2008).
17 D. A. Mercer, "Low-power approaches to high-speed current-steering digital-to-analog converters in 0.18-μm CMOS" *IEEE J. Solid-State Circuits* **42**, No. 8, 1688–1698 (Aug. 2008).
18 J. Savoj *et al.,* "A 12-GS/s phase-calibrated CMOS digital-to-analog converter for backplane communications," *IEEE J. Solid-State Circuits* **43**, No. 5, 1207–1216 (May 2008).
19 T.-M. Wang *et al.,* "On-glass digital-to-analog converter with gamma correction for panel data driver," *Proc. IEEE Intl. Conf. on Electronics, Circuits, and Systems,* 202–205 (2008).
20 M. Pelgrom, "A 50 MHz 10-bit CMOS digital-to-analog converter with 75 Omega buffer," *IEEE Intl. Solid-State Circuits Conf. Dig. Tech. Papers,* 200–201 (1990).
21 Y.-H. Tai *et al.,* "A statistical model for simulating the effect of LTPS TFT device variation for SOP applications," *IEEE J. Display Tech.* **3**, No. 4, 426–433 (Dec. 2007).
22 A. Hastings, *The Art of Analog Layout* (Prentice-Hall, Inc., 2001).
23 K. N. Leung *et al.,* "A 2-V 23-μA curvature compensated CMOS bandgap voltage reference," *IEEE J. Solid-State Circuits* **38**, No. 3, 561–564 (Mar. 2003).

Tzu-Ming Wang received his B.S. degree from the Department of Electronics Engineering, National Chiao-Tung University, Hsinchu, Taiwan, R.O.C., in 2005. He is currently working toward his Ph.D. degree at the Institute of Electronics, National Chiao-Tung University. His current research interests include analog circuit design on glass substrate and mixed-voltage I/O circuit design in low-voltage CMOS technology.

Yu-Hsuan Li received his M.S. degree from the Department of Electronics Engineering, National Chiao-Tung University, Hsinchu, Taiwan, R.O.C., in 2007. In 2007, he joined the Peripheral Circuit Design Department, System Technology Division, AU Optronics Corp. (AUO), as a Senior Engineer. His current research interests include sensing and low-power circuits integrated on panel for flat-panel-display applications.

Ming-Dou Ker received his Ph.D. degree from the Institute of Electronics, National Chiao-Tung University, Hsinchu, Taiwan, in 1993. From 1994 to 1999, he worked in the VLSI Design Division, Computer and Communication Research Laboratories, Industrial Technology Research Institute (ITRI), Hsinchu, Taiwan. Since 2004, he has been a Full Professor with the Department of Electronics Engineering and Institute of Electronics, National Chiao-Tung University, Hsinchu, Taiwan. From 2006 to 2008, he served as the Director of Master Degree Program at the College of Electrical Engineering and Computer Science, National Chiao-Tung University, as well as the Associate Executive Director of the National Science and Technology Program on System-on-Chip, Taiwan. In 2008, he was rotated to be a Chair Professor and Vice-President of I-Shou University, Kaohsiung, Taiwan. In the field of reliability and quality design for circuits and systems in CMOS technology, he has published over 370 technical papers in international journals and conferences. He has proposed many inventions to improve the reliability and quality of integrated circuits, which have been granted with 147 U.S. patents and 145 R.O.C. (Taiwan) patents. His current research interests include reliability and quality design for nanoelectronics and gigascale systems, high-speed and mixed-voltage I/O interface circuits, on-glass circuits for system-on-panel applications, and biomimetic circuits and systems for intelligent prosthesis. He had been invited to teach or to consult reliability and quality design for integrated circuits by hundreds of design houses and semiconductor companies in the worldwide IC Industry. He has served as a member of Technical Program Committees and the Session Chair of numerous international conferences. He also served as the Associate Editor for the *IEEE Transactions on VLSI Systems.* He has been selected as the *Distinguished Lecturer* in the IEEE Circuits and Systems Society (2006–2007) and in the IEEE Electron Devices Society (2008–2009). He was the President of Foundation in Taiwan ESD Association. In 2009, he was selected as one of the top ten *Distinguished Inventors* in Taiwan; and one of the Top Hundred *Distinguished Inventors* in China. In 2008, He has been elevated as an IEEE Fellow with the citation reading "for contributions to electrostatic protection in integrated circuits, and performance optimization of VLSI micro-systems."